A DISTRIBUTION SYSTEM

The present invention relates to a distribution system, and in particular a system for distributing video signals received on a digital video broadcast (DVB) interface, and a system for providing switched conditional access to the video signals.

A distribution system for video signals is described in International Patent Publication No. WO 97/09827, which is incorporated herein by reference. The system is able to receive video signals and then switch the signals to customers or subscribers. The system uses Digital Subscriber Line (DSL) transceivers to transport the video signals and POTS signals on copper lines between a telecommunications exchange and subscribers.

In accordance with the present invention there is provided a distribution switch for a local exchange, including:

an access unit for switching video channels transmitted to subscribers in response to channel requests received from subscribers; and

a control unit for controlling switching of the channels by the access unit in accordance with stored conditional access data.

The present invention further provides a distribution system for a local exchange, including:

a subscriber access system; and

a DVB interface unit having means for receiving DVB signals, means for extracting from the DVB signals a plurality of video channels, and means for multiplexing said video channels onto a data path for the subscriber access system.

Preferred embodiments of the present invention are hereinafter described, by way of example only, with reference to the accompanying drawings, wherein:

Figure 1 is a block diagram of a preferred embodiment of a distribution system;

Figure 2 is a block diagram of a distribution switch of the system;

Figure 3 is a block diagram of a distribution subrack of the distribution switch;

Figure 4 is a block diagram of a DVB channel interface unit of the distribution subrack;

Figure 5 is a block diagram of a switch conditional access system of the distribution system;

Figure 6 is a diagram of a conditional access process of the switch conditional access system;

Figure 7 is a diagram of the format of a conditional access message;

Figure 8 is a block diagram of an MPEG transport stream processor of the channel interface unit; and

Figures 9 and 10 are block diagrams of first and second parts of a multiplexer of the channel interface unit.

A distribution system 2, as shown in Figure 1, includes a plurality of distribution switches 4 located at local exchanges of the PSTN of a telecommunications carrier to connect subscribers or customers 6 to video information providers 8 or computer networks 10, such as the Internet or an office LAN. The distribution switch 4 includes ADSL transceivers for each subscriber 6 to establish communication channels with a respective ADSL transceiver 12 at the location of the subscriber 6. The communication channels include a high bit rate downstream channel, of about 6 Mb/s, a low bit rate bidirectional channel, of about 640 kb/s, and a channel for transmitting POTS signals. The subscriber transceiver 12 supports at least one television set top unit (STU) 14 for video programs, an Ethernet connection for a PC 16 and a telephone terminal 18 for the POTS signals. The downstream channel between the switch 4 and the subscriber 6 is primarily for downloading of video programs, whereas the low bit rate channel is primarily for control signals, such as program or channel selection signals sent by the subscriber 6 to the distribution switch 4. The distribution switch 4 establishes a bidirectional control channel with a video information provider 8, as required, and is able to receive high bit rate video signals downloaded on video feeds to the switch 4 from a video information provider 8.

The distribution switch 4, as shown in Figure 2, includes a distribution subrack 20 for receiving the video feeds from an inter-exchange network (IEN), such as an SDH or ATM network. The subrack 20 accesses or extracts the video channels from the video feeds and multiplexes them onto a data bus 24 for distribution to access subracks 26 of the switch 4. The access subracks 26 include ADSL transceivers and are able to select video channels from the bus 24 in accordance with subscriber requests and transmit the video channel data to subscribers 6 in the form of an ADSL signal. The access subracks 26 are able to perform channel switching for each subscriber 6. The access subracks 26 each include an integrated gateway unit (IGU) to receive control signals from the subscriber 6 and control channel switching.

The distribution subrack 20, as shown in Figure 3, includes a number of channel interface units (CIU) 30 for receiving the video feeds, and accessing and multiplexing the video channels in the feeds, a channel distribution unit (CDU) 32 for placing the multiplexed video channels onto the distribution bus 24, and an IGU 36 for handling control signals for the units 30 and 32.

Additional detail on the above components for the distribution system 2 is provided in International Patent Publication No. WO 97/09827, which is incorporated herein by reference.

A DVB channel interface unit 30, as shown in Figure 4, includes an MPEG2 transport stream processor 32 for receiving a 34.368 Mb/s DVB feed 34, and a multiplexer 36 connected to the output of the MPEG processor 32 for multiplexing the video channels extracted by the processor 32 into 34 bit data for the CDU 32. The CIU 30 further includes a PCR unit 38 connected to the processor 32, and a controlling CPU 39 to control the signal processing executed in the CIU 30. The CPU 39 also acts as a system information (SI) processing unit 40. The MPEG processor 32 demultiplexes the 34 Mb/s DVB feed 34 to extract up to 12 MPEG2 video channels, which are passed to the multiplexer 36, which multiplexes the channels into 34 bit data words. The DVB protocol is described in the

European Telecommunications Standards (ETS) 300-468, 300-421, 300-429, 300-472, and 300-473.

The MPEG processor 32 can select as its input feed 34 a G.703 serial input 42 or a parallel 8 bit data input 44. The 8 bit data input 44 is used to receive data from a QAM demodulator connected to a hybrid fibre coaxial (HFC) cable or to receive data from an STP-34 unit which converts 155 Mb/s SDH feed to 4 x 34 Mb/s data feeds. The MPEG processor 32 introduces packet jitter when the MPEG channels are output at fixed bit rates, and this jitter can be removed by signal processing in the set top unit, or alternatively the program clock reference (PCR) adjust module 38 can be added to eliminate the jitter by adjusting the PCR time stamps of each MPEG output stream. For channels or feeds which are encrypted by a video information provider, the PCR module or a substitute access module can be used to decrypt the MPEG stream. The SI processing unit 40 is a CPU which attends to processing of system information extracted from the DVB feed 34 by the MPEG processor 32.

A switched conditional access system 50 of the distribution system 2, as shown in Figure 5, includes a subscriber management system (SMS) 52 which is used to manage and set conditional access data to be sent to the distribution switch 4. The conditional access data includes content description data and subscriber entitlement data arranged in respective content description and subscriber entitlement tables. A content description table (CDT) relates to the content of the video channels delivered to the switch 4, and a subscriber entitlement table (SET) relates to the content which a subscriber is able to access from the switch 4.

The conditional access data is sent by the subscriber management system 52 to the IGUs 54 of the access subracks 26 of the distribution switch 4. The IGUs 54 constitute a level one (L1) gateway. The data can either be sent directly to the gateways 54 from the management system 52 using a management network path 56, or the data can be encapsulated in the DVB feeds 34 sent to the DVB CIUs 30. In the latter case, the content description and

subscriber entitlement tables are sent by the management system 52 to DVB encoders 58 for encapsulation with the video channels. The CIUs 30 then extract the tables and forward them via an Ethernet link 60 of the switch 4 to the gateways 54.

A content description table 62, as shown in Figure 6, includes for each type of content 65 on a channel received by the switch 4, a set of content descriptors 66 relating to the channel content. The descriptors 66 include program tiers relating to the type of program on the channel, a geographic mask designating geographic regions in which the program can be viewed, and any parental level or copy protection restriction information which can be used to provide further information on the program. A subscriber entitlement table 64 for each subscriber includes a tier descriptor designating the tier levels to which the subscriber can have access, a geographic descriptor, designating the geographic region of the subscriber, and an expiry date which specifies a date after which the subscriber is no longer allowed access. On receiving a request for a content channel from a subscriber, an IGU 54 accesses the subscriber entitlement table 64 for that subscriber and the content description table 62 for the program requested and compares the two to determine if the subscriber 6 is allowed to have access to the requested channel. Access is allowed, as shown in Figure 6, if:

(a) at least one of the tiers assigned to the program or channel corresponds to the tier level for the subscriber;

(b) the geographic region for the subscriber matches one of the geographic regions for the program or channel; and

(c) the current date 68 is less than the expiry date in the SET 64.

If the IGU 54 determines that access to the channel is allowed for the subscriber 6, it issues a control signal within the access subrack 26 to cause switching to the requested channel. The distribution system 2 can define 128 tiers. The parental level and copy protection data can be passed to the STUs 14 for display to the subscriber 6 or can be used at the STUs 14 to restrict access to certain classified programs. Access can also be restricted using this information at the distribution switch 4 by adding further corresponding data to the subscriber entitlement tables 64.

The SETs and CDTs are built in the switch 4 from transmitted sections. The sections that form the CDT are a program description section (PDS) and a tier description section (TDS). The SET is built from a subscriber entitlement section (SES). Several of each of the sections will typically be required to build an entire table. As stated above, the SETs and CDTs may be sent to the L1 gateways 54 either multiplexed onto a 34 Mbit/s MPEG-2 transport stream using the encapsulation described below, or directly sent using the management network.

The terms used below are referred to in the MPEG2 specification document "Information Technology General Coding of Moving Pictures and Associated Audio Information: Systems", ITU-T Recommendation H.222.0 (MPEG-2), International Telecommunication Union (Identical to ISO 13818-1).

The PDS, SES and the TDS share the same MPEG2 PID (packet identifier). The characters which make up the PDS, SES and TDS are encapsulated in MPEG2 PES packets of type 'private _stream_2' (stream_id in PES header = 0xBF) and identified within the program map table as 'PES packets containing private data' (stream_type in PMT = 0x06). In order to identify the private data stream containing the PDS, SES and TDS data, the DVB CIU 30 extracts the first stream identified by its PMT as having only this private data stream (i.e. no associated video or audio streams).

Due to an available interface into the MPEG encoder/multiplexer 58, the data stream between the SMS 52 and the DVB CIU 30 is an asynchronous character stream. Characters are sent to the multiplexer 58 at a maximum rate of 19.2 kbit/s. As characters arrive at the multiplexer 58, and depending on the currently available output bandwidth, one or more characters will be put into a PES packet (of stream_id = 0xBF) and inserted into the MPEG2 transport stream on the PID which has been set up for this data stream. It is possible for one PES packet to contain more than 178 characters, in which the PES packet would be sent in two or more MPEG2 transport packets. The 'payload_unit_start_indicator' bit is set in transport packets which contain the start of a PES packet. Transport packets in which the PES

packet does not completely fill the 184 byte data area are padded using an empty adaptation field. As there is no control of the number of characters in each PES packet, an asynchronous protocol is used to allow rapid message synchronisation. The encapsulation process is based on PPP in HDLC Framing, as described in Internet RFC 1549, Section 4, "Asynchronous HDLC".

Figure 7 illustrates the message format, which does not include start and stop bits, nor any characters inserted for transparency. The characters are transmitted from left to right. Another message may immediately follow the closing flag sequence of a message (i.e. two messages may share a common flag). Two consecutive flag sequences constitute an empty message, which is ignored, and not counted as a frame check sequence (FCS) error. Received frames with an incorrect FCS are discarded. The message field may hold one SES and one TDS or one PDS only. Multiple sections within a message are not allowed. The maximum length of the message field (including any characters inserted for transparency), which may be 230 characters, is governed by factors such as:

(i) Time to acquire the start of a message.

(ii) Probability of receiving a message without errors.

(iii) Efficient use of transmission bandwidth.

There are no address and control fields, as are traditionally used in HDLC links. As defined in PPP in HDLC Framing, Internet RFC 1549, Section 3.2, these can be omitted to conserve bandwidth.

All characters are transmitted with eight significant bits of data, and the flag sequence indicates the beginning or end of a message. The character stream is examined on a character-by-character basis for the value of 01111110 (0x7e). The frame check sequence field is defined to be 16 bits (two characters). The FCS is transmitted with the coefficient of the highest term first. The FCS field is calculated over all bits of the message, not including start and stop bits nor any characters inserted for transparency. This does not include the flag sequences nor the FCS field itself. The end of the message is found by locating the closing flag sequence and removing the frame check sequence field. The specification for the FCS is

described in ISO 3309 or ITU X.25. A character stuffing procedure is used to allow transparency. The control escape character is defined as binary 01111101 (0x7d).

The DVB CIU 30, as described previously, supports a number of network interface modules (NIMs):

(a) a 34 Mbit/s G.703 NIM 42.

(b) a 16/64 QAM NIM 44.

The CIU 30 has the following inputs, as shown in Figure 8:

(i) A 34 Mbit/s input parallel 74 from an STP-34 SDH demux unit. The STM-34 unit converts an STM-1 155 Mb/s feed to 140 Mb/s and then demultiplexes this signal to 34 Mb/s.

(ii) Parallel 8 bit input 72 which is unscrambled data from an integrated receiver decoder (IRD), a QAM NIM 44, or a QPSK NIM.

(iii) A G.703 serial input 70.

When the STP-34 SDH input 74 is used, the 34 Mbit/s G.703 NIM 42 performs Reed-Solomon forward error correction (FEC). The 34 Mb/s input signal is processed as described below.

The received HDB3-coded input signal 70 is converted to the NRZ signal format. The signal is then converted to a parallel format and fed to a Reed-Solomon chip (L64705) 76 with the input 74. A Viterbi Decoder of the FEC chip 76 is configured in the bypass mode. In this mode the input to the FEC chip is in the form of 8 bit parallel decision bytes. A field programmable gate array (FPGA) on the NIM card 42 synchronises the input stream and converts it to 8 bit parallel data. An access (CA) port 78 is available after the FEC chip 76 for the PCR module 38 or the access module, discussed previously. The CA port 78 provides access to all of the incoming streams within the MPEG2 transport stream for decryption, if necessary.

MPEG2 transport stream lock is found by a lock unit 80. The PID location is found, and a dual port select signal CK4 is generated from the 24 MHz master clock. This signal goes low for one clock cycle for every MPEG data byte being input into a main FIFO 82 by the stream processor 32. When this signal is high the stream outputs data from the FIFO 82 and the CPU 39 can access the data.

Incoming data is stored in 8 bit parallel form in a 16 Kbyte RAM FIFO 82 with packet alignment within 256 byte blocks. Accesses to this FIFO 82 occurs at a cycle rate of 24 MHz. This dual-ports the RAM with an effective input rate of 34 Mb/s and a maximum output rate of 158 Mb/s (three times the input rate). Writes to the FIFO occur when CK4 is low and reads occur when CK4 is high.

If the PCR module 38 is included, an incoming packet is time stamped with a 27 MHz/300 counter values in place of the MPEG2 sync information, which is used for PCR adjustment. Due to the packet alignment procedure the sync information is no longer required. Sync is reinserted by the PCR module 38 as the data is transferred to the bus multiplexer 36.

When the PID number is received it is used to address an 8 Kbyte x 13 bit look-up table 86 (comprising 12 output streams and one CPU access stream). Each output bit allows a particular packet to be sent to the corresponding output stream. SI information packets have all output bits set, as all streams contain these packets.

When a packet is to be sent to a particular output stream its address within the 16 Kbyte main FIFO 82 is stored in a packet FIFO 84. The address is the packet # which can range from 1 to 63 which is obtained by the packet counter 81. There are 12, 16x6 bit packet FIFOs 84. After a packet has been transferred to the output stream its address is cleared and the next packet address is read. If the next input packet is not yet available then the packet address is still zero and a null padding cell is sent. Packet address = 0 points to a null cell in the main FIFO 82. If the input rate for a particular stream is higher than the output rate then the packet address which is overwritten will be non-zero. This produces a CPU interrupt

and the CPU 39 can then assign a higher output rate to that stream. The input data rate of a particular stream can be selected and measured by the CPU 39.

Two modes of operation allow the output rates to be limited to either 6.608 Mb/s and 3.304 Mb/s or 6.312 Mb/s. All streams at a particular rate are synchronous.

Based on these clock rates two types of data request (data request frequency = clock /8) are sent from the bus multiplexer 36 to two address counters 83 which share the output side of the main FIFO. The first stage of these counters 83 divide by 188. The second stage counts modulo 16 packets which point into the flow FIFO. Each output stream is serviced with the correct address (8 bits) specified by its assigned bit rate. However each stream has an independent packet address as stored in its flow FIFO 84. A stream sequence counter 88 makes sure that each stream is serviced in turn. A mode RAM 90 stores the bit rate associated with each stream and this selects the appropriate address counter 83.

To make sure that each stream is only serviced once, two 16 cycle one-shot circuits 85 are connected to the data requests 87 from the bus multiplexer 36. Only a particular stream is serviced once while the output from the one-shot circuit 85 is active. The output of the circuits 85 are combined with the stream sequence count to indicate that valid data is present for a particular stream.

Data is transferred bytewise to the bus multiplexer 36 from the main FIFO 82 when the write enable (WE) signal 89 is active for a particular stream address 91.

To process SI data the 13th packet FIFO 84 is used. The stream processor 32 selects PIDs that contain SI data. Data is transferred to the CPU 39 without the insertion of null cells. A bit is set to indicate a packet is present and the CPU 39 can then read it from the FIFO 82. Hardware DMA support is available if program transfer rates are inadequate. Null cell pointers are not entered into the packet FIFO 84 because the CPU polls the availability of a packet.

The main FIFO RAM 82 is initialised with a null cell by writing to the transport stream processor 32. The CPU access removes a clock from the dual port select signal and this clock cycle is used to write CPU data to the FIFO 82.

The PCR module 38 ensures time alignment between the PCR time stamp for the output stream and the time when it is sent to the multiplexer 36. The PCR module 38 modifies the bit stream on the 8 bit data bus 93 to the multiplexer 36.

The bus multiplexer 36, as shown in Figures 9 and 10, includes a conversion FPGA 101 and a multiplexing FPGA 103.

The conversion FPGA 101 supplies data request signals 87 at the byte rates of the 3M and 6M streams to the transport stream processor 32. The transport stream processor 32 generates the FIFO clock, the WE signal 89 and four qualifying address signals 91. There are twelve 8 bit latches 100 and during one byte period of the 3M stream one byte of data is latched into each latch which is handling a 3M transport stream and 2 bytes are latched in each 6M latch.

The latch outputs are serialised to provide 12 bit streams, each of which may be either a 6M or a 3M channel. All channels at a particular bit rate are synchronous.

By using fixed bit-stuffing to reduce the data rate, each 6M channel is split into four 2.10625 Mbps streams and each 3M channel is split into two 2.10625 Mbps streams. Variable bit-stuffing is also performed to synchronise each channel with a 2.10625 MHz clock derived from the 33.7 MHz system clock. The output of the conversion FPGA 101 comprises 48 x 2.10625 Mbps (12x4x2.10625 Mbps) streams 102. Four of the streams 102 can represent either a 6M or a 3M channel. If it is 6M, four streams, TS1, TS2, TS3 and TS4 are used, while in the 3M case only two streams, TS1 and TS2 are used and the other two remain unused in each group of four.

Each of the 48 streams 102 from the conversion FPGA 101 is fed to the multiplexing FPGA 103, along with 'b0_valid'. 'b0_valid' is the variable-stuffing-bit flag associated with TS1, and allows the original bit stream to be recovered later in the system. As each stream 102 is clocked into the multiplexing FPGA 103, a serial calculation of parity is performed over each group of 32 successive data bits (which will eventually form a 32 bit parallel data word) plus 'b0_valid'.

For each of the twelve groups of four streams, TS1, TS2, TS3 and TS4, there are two memory banks 104, each comprising 34x12 bit RAMs. One memory bank is filling while the other is outputting its data.

When the data is read out of the memory, all 32 data bits for a given channel (plus 'b0_valid' and 'parity') are read out simultaneously as a parallel data word. Parallel data words are read out in order for channels 1 to 12. For each channel, streams TS1, TS2, TS3 and TS4 are all read out of memory simultaneously at a rate of 8.425 MHz, and are then multiplexed together at a 33.7 MHz rate, so that at the FPGA 103 output terminals data words appear in the following order (in the case of a 6M stream) ..... Ch1 TS1, Ch1 TS2, Ch1 TS3, Ch1 TS4, Ch2 TS1, Ch2 TS2, Ch2 TS3, Ch2 TS4, ...

In this way, the 48 x 2.10625 Mbps transport streams (corresponding, for example, to 12 x 6M streams) are time division multiplexed (TDM) sequentially onto the internal data bus, along with the stuffing flag and a parity bit, resulting in a 34 bit bus 31.

During each frame, each DVB unit 30 outputs 48 parallel data words on the bus 31 to be multiplexed onto the TDM bus 24 by the CDU 32. The time at which each DVB unit 30 outputs its data is controlled by active-low 'Select' lines from the CDU 32. These lines change state on positive edges of the system clock, and each DVB CIU 30 begins to output its data on the positive clock edge immediately following the positive edge at which its 'Select' line went low.

When ATM video is transported to subscribers, the conversion FPGA 101 includes circuitry for each channel to adapt the MPEG2 transport packets to ATM 53 byte cells according to the AAL5 standard. The multiplex FPGA 103 transfers these ATM cells directly to the CDU 32 for transmission on the data bus 24.

Although all DVB CIUs 30 operate off a 33.8 MHz system-clock, the clocks to pairs of subracks are staggered by 180°. The CDU 32 reads data from one subrack of the pair during the first half of the 33.7 MHz cycle, and from the other subrack during the second half of the cycle. In this way a word rate of 67.4 MHz is obtained at the CDU 32, while each DVB CIU 30 operates at 33.7 MHz.

Error-rate monitoring, signal-loss detection and MPEG detection are provided for the input channel.

A loop-back circuit 105 is provided which routes any chosen bearer back to a diagnostic port for fault detection and testing. The bearer can be looped-back at the line interface, the output of the conversion FPGA 101, or the output of the multiplexing FPGA 103.

The reference clock can be slaved from an external clock source via the PCR module 38. Internal clock operation is provided in event of failure.

When installed the PCR module 38 pulls the PCR-present signal to ground. This informs the stream processor 32 to insert arrival time stamps. The PCR module provides the 90 KHz clock (27 MHz/300) clock reference 95 for these time stamps. A terminal count (TC) signal from the PCR to the PCR module allows the stream processor 32 to synchronise its time counter.

The PCR module 38 corrects the PCR information within MPEG2 packets at the output of the stream processor 32. Without the PCR module 38 installed the data lines are

connected directly between the processor 32 and the multiplexer 36. The PCR module introduces an 'N' clock delay to the data path. To maintain proper bus multiplexer operation the stream # address and the WE signal are delayed by 'N' cycles.

A time stamp indication, which is coincident with the start of the packet, is available from the stream processor 32. The PCR module continually inserts a '0x47' to replace the time stamp on the output of the data to the bus multiplexer 36.

The PCR module 38 subtracts the current time from the time stamp recovered from the stream to obtain a time difference. It then waits for the actual PCR information embedded in the MPEG2 stream. It adjusts this information with the time difference previously measured. In this way jitter introduced by the stream processor 32 can be removed. This function is performed for each of the 12 output streams from the stream processor 32.

The PCR module 38 has access to the data bus of the CPU 39 and may be configured and monitored by the CPU 39.

The CPU 39 is provided by a Motorola 68360 microprocessor which supervises the operation of the CIU 30. The microprocessor 39 gathers and processes the SI data, alarm, error and status information and communicates these to the IGU 36. The CPU 39 is also responsible for configuring the FPGAs 101,103 of the bus multiplexer 36 and FPGAs of the PCR module 38 and the stream processor 32.

Many modifications will be apparent to those skilled in the art without departing from the scope of the present invention as herein described with reference to the accompanying drawings.